# High-Efficiency Buck Converter for Notebook Computers

## INTRODUCTION

Today, the untethering of electronic equipment has given rise to the need for lightweight power sources and power regulation. Extremely efficient buck converters answer one part of this need. The low losses of these converters eliminate the need for heavy heat sinks and power device packaging. In addition, the energy that is normally consumed by the power converter is available for the application.

In this application note, we present a dc-to-dc converter which is intended for use in notebook computers and other portable products. This converter is designed for maximum efficiency, which is made possible by two innovations-lossless current sensing and synchronous rectification. The converter is rated for a load current of 1.5 A and achieves a maximum efficiency of 94% while producing 400 mA at 3.3 V with input voltage of 6 V. The same design was also configured to produce 5 V. 97% efficiency was achieved with input of 6 V, output of 5 V, and output current of 400 mA. The total PCB area is about 2.25 in.$^2$, with a height of 0.25 in. All components except the inductor use surface-mount packages. Furthermore, there are no lead-formed TO-220s or DPAKs, which results in very light weight and small size.

## Si9150CY IC DESCRIPTION

The Si9150CY is a BiCMOS PWM controller IC with all active components necessary for a synchronous buck converter. It is designed to be used with the LITTLE FOOT® series of low-voltage MOSFETs.

By using higher cell densities (2.5 to 3 million cells per square inch), both the high-side MOSFET switch and the synchronous rectifier (SR) can be housed in a single 8-pin small-outline IC package. While an n-channel MOSFET is the obvious choice for the ground-referenced SR, either p- or n-channel MOSFETs can be used for the high-side switch. N-channel MOSFETs require charge pump and/or bootstrap circuits to generate sufficient gate voltage for channel enhancement. P-channel devices are simple to drive but have higher on-resistance for a given die size. Because of recent improvements in p-channel MOSFET designs, the p-channel approach was chosen for its simplicity. The Si9943 includes a 160-mΩ p-channel and a 100-mΩ n-channel MOSFET in an SOIC-8 package. The Si9150CY controller is housed in a 14-pin SOIC.

Since a pin-by-pin description of the Si9150CY is included in its data sheet, we limit this discussion to some interesting details of the functional blocks.

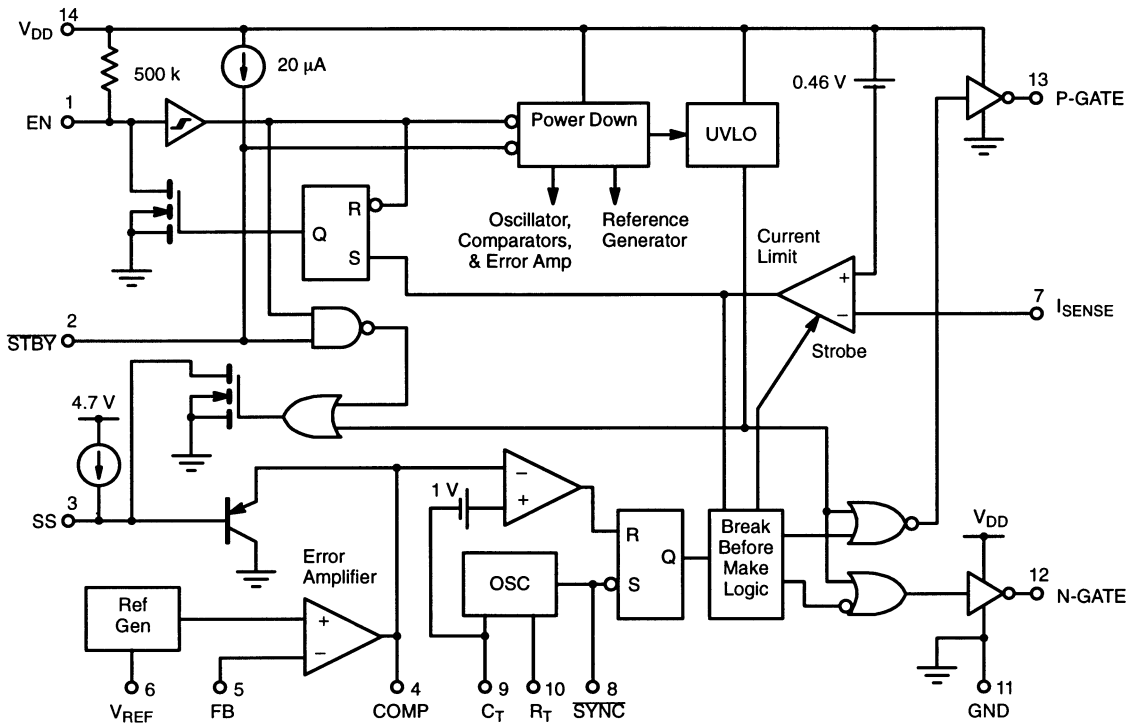



**FIGURE 1.** Si9150CY Block Diagram

## BREAK-BEFORE-MAKE

To prevent shoot-through it is essential to turn off one MOSFET before turning on the opposing MOSFET. The Si9150CY senses the voltages on the N-GATE and P-GATE pins. N-GATE will not be pulled high until P-GATE is within a few volts of $V_{DD}$. Likewise, P-GATE will not be pulled down until N-GATE is a few volts above GND. The thresholds are determined by using asymmetrical CMOS inverters, i.e., one transistor is significantly larger than the other, so that the logic threshold becomes the gate-to-source threshold of the larger device. There is also a delay while the signal, once enabled, is buffered by the output drivers. This delay is typically 75 to 100 ns. The total deadtime (both MOSFETs off) is equal to about 150 ns.

## CURRENT LIMIT

The current limit is a strobed slow-acting comparator which monitors the drain of the p-channel MOSFET. It is triggered when the voltage on the $V_{DD}$ pin minus that on the $I_{SENSE}$ pin is greater than 0.46-V typical, provided that the P-GATE pin has been pulled below about 1.5 V. Once the current limit is triggered, the EN pin is pulled low until the IC shuts down, resetting the dc-to-dc converter and the current limit. The comparator is relatively slow, allowing about 400 ns for the system to settle down after the p-channel MOSFET has turned on. Once the p-channel MOSFET is driven on, it appears in the circuit as a drain-to-source resistance. By using this resistor to sense the current, additional resistors or current transformers are eliminated. This reduces both cost and losses, making it possible to achieve extremely high efficiency. It does, however, restrict the current limit trip point, which is now determined by the MOSFET on-resistance.

## OSCILLATOR

The oscillator works by applying 2.5 V to the $R_T$ pin. The current flowing out of the $R_T$ pin is mirrored and fed into the $C_T$ pin. When the $C_T$ pin reaches 2.5 V, an internal MOSFET pulls the $\overline{\text{SYNC}}$ pin low. The low voltage on $\overline{\text{SYNC}}$ causes the $C_T$ pin to be pulled low, resetting the clock. Allowing for small offset voltages, the frequency, f, is

$$f = \frac{0.9}{C_{OSC} \times R_{OSC}} \quad (1)$$

where $C_{osc}$ and $R_{osc}$ are the capacitor and resistor values tied to the $C_T$ and $R_T$ pins, respectively.

The $\overline{\text{SYNC}}$ voltage is also passed through three inverters to square the edges, and the signal is used to reset the PWM circuitry in the IC. Since the clock resets whenever the $\overline{\text{SYNC}}$ pin is pulled low, two Si9150CYs can be synchronized by connecting their $\overline{\text{SYNC}}$ pins together. If synchronization to an external clock is desired, $\overline{\text{SYNC}}$ should be pulled low for a short period using a 2N7002 or similar MOSFET. The recommended reset pulsewidth is approximately 100 ns.

## REFERENCE GENERATOR

The reference generator is a temperature-compensated bandgap, which is powered whenever the EN pin is high. The output from the bandgap is run through a trimmed voltage divider to an amplifier that can source about 10 mA to the $V_{REF}$ pin. If more than 10 mA is drawn from the amplifier, it will shut down momentarily.

The sink current capability is only about 100 µA, however. Since the reference has available more than a hundred times as much pull-up as pull-down current, noise on the power pins is effectively rectified. When this happens, either a dc voltage higher than 2.5 V or a relatively low-frequency sawtooth is present on the $V_{REF}$ pin. Since this voltage is used in all parts of the IC, it will not perform to specification if the reference is out of specification. We recommend bypassing the $V_{REF}$ pin with a minimum capacitor value of 0.1 µF to ground.

## POWER DOWN

The power down section of the IC is a group of load switches and switchable current mirrors. With the EN pin high and the $\overline{\text{STBY}}$ pin low, only the reference generator, the UV lockout, and the pull-up for the $\overline{\text{STBY}}$ pin will operate. With both the EN and the $\overline{\text{STBY}}$ pins high, all other systems are switched on. With EN pulled low, only the EN pull-up resistor consumes power.

Under very low load conditions the efficiency of switch mode power converters decreases very rapidly. When it is desirable to operate under light load (<50 mA) for an extended period of time it may be beneficial to implement a linear regulator. With $\overline{\text{STBY}}$ low and EN high, the Si9150CY provides the voltage reference needed for implementation of a linear regulator.

## DESIGN EXAMPLE

The dc-to-dc converter shown in Figure 2 is designed especially for use in notebook computers. With a 6-, 8-, or 10-cell NiCd battery to power the computer, it is necessary to convert a variable voltage to 5 V and 3.3 V.

We assumed the use of two converters, one for each output voltage. This duplication increases the component cost somewhat but allows simple implementation of independent regulation and current limits. A typical computer would use about 500 mA at each voltage, but at times would need up to 1.5 A. While weight and efficiency are optimized, cost effectiveness is also kept in mind. The 5-V converter is considered in depth because, in many respects, it is more difficult to design. In order to reconfigure the resulting converter for a 3.3 V output, it is necessary merely to change R4 to 105 kΩ.

## CONVERTER SPECIFICATION

The specifications given in Table 1 are representative of a typical portable application. The current limit has been specified fairly loosely, because most applications will permit it and because the lossless current limit circuit requires a wide current limit spread.

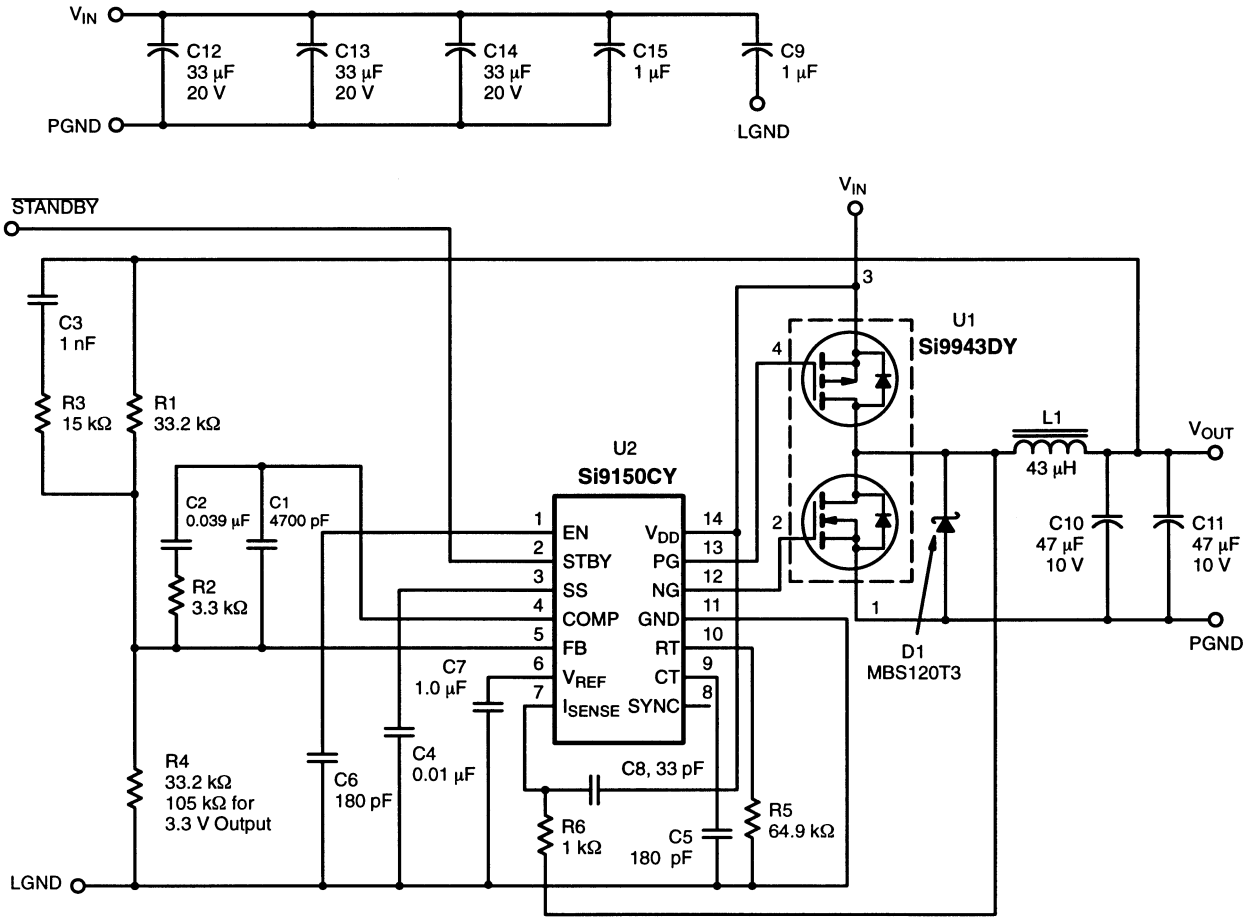



**FIGURE 2.** 5-V Synchronous Buck Regulator Schematic

**TABLE 1.** DC-to-DC Converter Specifications

| Spec | Typ | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| $I_{max}$ | | 1.5 | | A | |
| $I_{CL}$ | 2.1 | 1.5 | 5.7 | A | $T_J$ < 150°C under fault conditions |
| $I_{no\ load}$ | 4 | | 8 | mA | |
| $I_{shutdown}$ | 300 | | 500 | µA | |
| $V_{in}$ | 10 | 6 | 16.5 | V | |
| $V_{out}$ | 5 | 4.85 | 5.15 | V | |
| Step-load | 150 | | 300 | mV | $I_{out}$ 10% to 90% |
| Output ripple | 40 | | 100 | $mV_{rms}$ | $V_{in}$ = 16.5 V |
| Input ripple | 300 | | 400 | $mV_{rms}$ | $V_{in}$ = 16.5 V, $I_{out}$ = 1.5 A |
| Start time | 2 | 1 | 5 | ms | |
| Efficiency | 97 | 94 | | % | $I_{out}$ = 0.5 A |
| Operating temp | 25 | 0 | 50 | °C | |
| Switching frequency | 76 | 65 | 85 | kHz | |

$I_{no\ load}$ is the maximum current that is permissible for the unloaded converter to consume while operating. But this level is too high for a typical computer's shut-down mode, so a linear regulator or small bang-bang converter is assumed to supply power while the computer is shut down. The $I_{shutdown}$ specification is important during this time. $I_{max}$ is the current that the load needs to operate. (Actually, this specification is redundant with minimum $I_{cl}$, but we include it here for clarity.) The maximum current limit trip point must occur at a current that does not cause safety concerns. Likewise, the output voltage must be within the operating voltage requirements of the load. For most 5-V circuitry, this is 5 V ±10%. This range must be padded to account for voltage drops and noise generated in the load. The deviation from 5 V can be broken down into dc accuracy, noise, and step-load response. Since, in most designs, the load will not jump from 10% to 90% in a few microseconds, the step-load figure may be divided in half. The load's decoupling capacitors and trace resistances provide an RC filter which smooths the output voltage, allowing the RMS value for output ripple voltage to be used. Thus, the sum of the dc error, half of the step-load response, and the RMS ripple should be less than or equal to about 8% of 5 V. The above explanation is based on rules of thumb and should be scrutinized by the system designer before use. The safest specification uses peak ripple and full step response. Also note that the converter will tend to run a few degrees above the ambient temperature, and it will not be operated while the computer is outside its temperature range.

## DESIGN METHODOLOGY

A description of the buck converter design procedure is given here. This particular design employs the Si9150CY driving the Si9943DY complementary half-bridge, but other converters can be designed using the same method.

The first step in designing with the Si9150CY is to choose the p-channel MOSFET switch to meet the load current requirements. $r_{DS(on)}$ variations over the spec ranges for voltage and temperature will affect the output current limit trip point, $I_{CL}$, since $r_{DS(on)}$ is used as the current sensing resistor. Once it is verified that maximum load requirements can be met, the inductor can be designed to meet efficiency and size requirements. In the discussion below, the ripple and power losses are calculated for the surface-mount tantalum capacitors, and some criteria are given for selection of the Schottky diode. An explanation of the feedback network is given, and finally soft-start capacitor selection and board layout considerations are discussed.

## WORST-CASE CURRENT LIMIT CALCULATIONS

There are three important current limit values that must be considered when choosing the p-channel MOSFET. First, the minimum current at which the current limit will trip ($I_{CLmin}$). This value is needed to ensure that the converter will power the load under all conditions. Secondly, the maximum current at which the current limit will trip ($I_{CLmax}$). This value is needed to satisfy safety and system specifications, as well as for inductor design. Finally, the maximum current ($I_{CLtherm}$) with the MOSFET's junction at its maximum rated temperature is needed to verify the converter's ability to survive a short circuit under worst-case conditions.

The current limit will trip if the voltage across the p-channel MOSFET is more than $V_{CL}$ while the MOSFET is fully on. The peak drain current is the sum of the average inductor current and one half the ripple current. Therefore,

$$I_{CL} = \frac{V_{CL}}{r_{DS(on)}} - \frac{I_{ripple}}{2} \quad (2)$$

The values of $V_{CL}$, $r_{DS(on)}$, $T_J$, and $I_{ripple}$ that are used to calculate each of the current limit ratings are given in Table 2. Unfortunately, the equations for these parameters are non-linear and interdependent. Therefore, an iterative approach is needed, consisting of the following steps.

**TABLE 2.** Worst-case Parameters as Used for the Current Limit Calculations

| Type | $V_{CL}$ | $r_{DS(on)}$ | $T_J$ | $I_{ripple}$ |
|---|---|---|---|---|
| $I_{CLmin}$ | Min | Max | Max | Max |
| $I_{CLmax}$ | Max | Min | Min | Min |
| $I_{CLtherm}$ | Max | Min | Max | Min |

Begin by estimating $T_J$ = 150°C at $V_{in}$ = 16.5 V and assuming $I_{ripple}$ = 0, so that $r_{DS(on)}$ can be determined. Calculate the power dissipation, including switching and conduction losses. Iterate the calculations to find the correct $T_J$. Determine the allowable ripple for $I_{CLmin} \geq I_{out(MAX)}$ = 1.5 A, which yields the minimum value for L. Having found L, use $r_{DS(on)}$ and $T_J$ to verify operation at $I_{CLmin}$ and $I_{CLtherm}$.

Power dissipation comes from two sources—switching losses and conduction losses. The conduction losses are equal to the square of the RMS current times the $r_{DS(on)}$ of the MOSFET. Assuming that the inductor is operating in its linear region and that the converter is efficient, the current running through the p-channel MOSFET is given by equation 3.

$$I_P(t) = \frac{V_{in} - V_{out}}{L} \times t + I_{out} - \frac{I_{ripple}}{2} \quad (3)$$

where $I_p(t)$ is the current through the p-channel MOSFET, $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $I_{out}$ is converter output current, L is the inductance in Henries, and $I_{ripple}$ is the inductor peak-to-peak ripple current. t is 0 when the p-channel MOSFET turns on and, t is $I_{ripple}$ times L divided by the quantity $V_{in}$ - $V_{out}$ when the MOSFET turns off. The RMS current through the MOSFET ($I_{rmsp}$) is given by

$$I_{rmsp} = \sqrt{\left[I_{out}^2 + \frac{I_{ripple}^2}{12}\right] \times \frac{V_{out}}{V_{in}}} \quad (4)$$

Conduction loss ($P_{conp}$) can now be calculated.

$$P_{conp} = r_{DS(on)} \times \frac{V_{out}}{V_{in}} \times \left[ I_{out}^2 + \frac{I_{ripple}^2}{12} \right] \quad (5)$$

Energy lost per switching transition may be approximated by

$$E_{swp} = V_{in} \times I_P \times t_f \quad (6)$$

Here, $t_f$ is the equivalent switching time for the MOSFET. A conservative number to use with the Si9943DY is 80 ns. This number will scale with gate charge, $q_G$, if other MOSFETs are used. Including both transitions, switching losses ($P_{swp}$) can be calculated using equation 7.

$$P_{swp} = 2 \times V_{in} \times I_P \times t_f \times f \quad (7)$$

where f is the clock frequency. The total power dissipated by the p-channel MOSFET is

$$P_p = P_{conp} + P_{swp} \quad (8)$$

To calculate allowable $I_{ripple}$, the $I_{CLmin}$ specification must be recalculated using the calculated value for $T_J$. Using

$$T_j = P_p \quad R_{thJA} + T_a \quad (9)$$

the equations for $P_p$, frequency (76kHz), and the graph of normalized $r_{DS(on)}$ versus $T_J$, an estimated $T_J$ may be calculated. Here $T_a$, the ambient temperature, is 50°C, and $R_{thja}$, the junction-to-ambient thermal resistance, is assumed to be 62.5°C/W. After a couple of iterations, $T_J$ is 90.7°C and $I_{CLmin}$ is 2.02 A. This allows a maximum $I_{ripple}$ of 1.0 A. Using the equation for $I_p(t)$ above,

$$I_{ripple} = \frac{(V_{in} - V_{out}) \times V_{out}}{f \times L \times V_{in}} \quad (10)$$

Therefore, this ripple current corresponds to an inductance of 43 µH with the worst case $V_{in}$ = 16.5 V.

Now that the limits of the ripple current are known, the survivability of the converter can be checked for $r_{DS(on)}$ values corresponding to both $V_{in}$ = 6 V and $V_{in}$ = 16.5 V. Using equation 9 for $T_J$ and the graph of $r_{DS(on)}$ versus $T_J$, the actual $T_J$ and $I_{CLtherm}$ are calculated.

**TABLE 3.** Calculated Worst-case Current Limits Including Temperature and Ripple Current Effects

| Spec | $V_{in}$ | Inductance | Current | $T_j$ |
|---|---|---|---|---|
| $I_{CLmin}$ | 6 V | Large | 1.62 A | 91°C |
| $I_{CLmin}$ | 6 V | 43 µH | 1.53 A | 86°C |
| $I_{CLtherm}$ | 6 V | Large | 2.89 A | 141°C |
| $I_{CLtherm}$ | 6 V | 43 µH | 2.76 A | 134°C |
| $I_{CLmax}$ | 16.5 V | Large | 5.6 A | N/A |

When used together, the Si9943DY and Si9150CY produce a converter which can be counted on to produce 1.5 A and which will tolerate any overcurrent situation which might arise. For operation above 13.5 $V_{DD}$ a filter (1 kΩ, 33 pF) is needed between the MOSFET drains and the $I_{SENSE}$ pin, refer to Figure 2.

## INDUCTOR DESIGN

Having selected the p-channel MOSFET and determined the ripple current and the minimum current at which the inductor can be fully saturated, the inductor and other power components may be selected.

The inductor must meet five criteria:

1. Inductance of more than 43 µH
2. Linear while current is in the converter's operating range
3. Not fully saturated at a current of $I_{CLmax}$
4. Low cost and small size
5. Acceptable efficiency

To meet all of these criteria, a conveniently sized core is chosen, and the efficiency of the resulting inductor is checked. If the efficiency is acceptable, the design is done. If not, the inductor's size is adjusted until acceptable efficiency is reached. An approximate size and type of material must be chosen. Usually, either MPP or a power ferrite with an air gap is used in this type of application.

In this example, an MPP toroid will be used. The following values are needed-inductance (L), the peak magnetic field at which the core material is linear ($B_{pk}$), the peak current at which the inductor is linear ($I_{pk}$), the core equivalent length ($l_e$), the core equivalent cross section ($A_e$), and the available core permeability values. Using cgs units, the inductance is

$$L = \frac{4 \times \pi \times A_e \times N^2}{l_e} \times 10^{-9} \quad (11)$$

where π is 3.14 and N is the number of turns. Also, using the following relationships,

$$n = \frac{N}{l_e} \tag{12}$$

$$H_{pk} = \frac{4 \times \pi \times n \times I_{pk}}{10} \tag{13}$$

$$\mu = \frac{B_{pk}}{H_{pk}} \tag{14}$$

the maximum value of μ can be determined from

$$\mu_{MAX} = \frac{A_e \times l_e \times B_{pk}^{\ 2}}{4 \times L \times \pi \times I_{pk}^{\ 2}} \times 10^{-7} \tag{15}$$

A Magnetics Inc. MPP core size of 55040 is larger than necessary, so the 55290 size is checked. Under normal operation the inductance should remain constant, so use $I_{pk}$ = 3 A. Since MPP has a soft saturation characteristic, it may be used aggressively, and $B_{pk}$ = 5500 gauss is chosen. If a ferrite is used, $I_{pk}$ = 5.7 A and the ferrite's $B_{sat}$ at 150°C would be used to prevent complete saturation under worst-case conditions.

The gap can be adjusted to give the desired equivalent permeability. An ungapped ferrite should not be used. The 55290 core has $A_e$ = 0.095 $cm^2$ and $l_e$ of 2.18 cm. Plugging these numbers and 43 μH into the above equation, $\mu_{max}$ is 131. Referring to the catalog, 125 is the next lower permeability available. Using the above equations,

$$N \le \frac{10 \times l_e \times B_{pk}}{4 \times \mu \times \pi \times I_{pk}} \tag{16}$$

If μ = 125, N is less than 25.4 turns. Using a 55290 core with 25 turns and the equation for L above, L is 42.7 μH. Since there is some leeway in the $I_{CLmin}$ specification, this value is acceptable.

Now, losses in the inductor are calculated. While the p-channel MOSFET is on, the current in the inductor is the same as the current through the p-channel MOSFET. When the MOSFET is off, the current ramps back down to the same level as at t = 0. Thus, the inductor RMS current ($I_{rmsi}$) can be calculated as

$$I_{rmsi} = \sqrt{I_{out}^{\ 2} + \frac{I_{ripple}^{\ 2}}{12}} \tag{17}$$

The resistance of the inductor wire equals the wire length times its resistance per unit length, which for 25 turns of 24-gauge copper wire is

$$R_W = 0.839 \frac{m\Omega}{cm} \times 48 \text{ cm} = 40 \text{ m}\Omega \tag{18}$$

Next the wire losses ($P_{wire}$) in the inductor can be calculated. Since the converter will typically run at less than 1 A, $I_{out}$ has been set to 1 A.

$$P_{wire} = I_{rms}^{\ 2} \times R_W = 40 \text{ mW} \tag{19}$$

or about 0.8% of the output power. Finally, core losses are calculated. The ripple in the B field (ΔB) is given by

$$\Delta B = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f \times N \times A_e \times V_{IN}} \times 10^8 \tag{20}$$

Substituting $V_{in}$ = 10 V (the input voltage at which the inductor voltage is a symmetric square wave), ΔB = 1,238 gauss. Using the equation supplied by the core vendor, the loss is

$$P_{core} = 0.489 \times 10^{-11} \times 0.0039 \times f^{i.28} \times \left(\frac{\Delta B}{2}\right)^{2.14} \tag{21}$$

or 37 mW. Although this number is not exact, it is evident that core losses are not a problem. The total loss due to the inductor is about 1.5% of the output power-small enough for this application.

## CAPACITOR SELECTION

If the load and source capacitances are ignored, the minimum capacitance and maximum ESR values are obtained, which may be used for conservative design. Such an approach leads to overdesign. Instead, the input capacitor was chosen to avoid significant losses or voltage drop, and the input and output capacitor ESR values are assumed to be halved by the power source and load capacitors. 33-μF, 20-V and 47-μF, 10-V tantalum capacitors are checked for the input and output filters. Three capacitors are paralleled for the input, and two for the output. After halving, the maximum rated ESR for AVX surface-mount capacitors are 166 mΩ and 225 mΩ for the input and output, respectively.

Although the ripple voltage is usually the limiting factor, the power dissipated in the capacitors will be discussed first. The current flowing through the input capacitor ($I_{cap}$) is

$$I_{cap}(t) = I_P(t) - \overline{I_P(t)} \tag{22}$$

where $I_P(t)$ is the current through the p-channel MOSFET and $\overline{I_P(t)}$ is the average input current. The input capacitor RMS current ($I_{rmsci}$) is

$$I_{rmsci} = \sqrt{\overline{I_P^2(t)} - \overline{I_P(t)}^2} \quad (23)$$

or

$$I_{rmsci} = \left[ I_{out}^2 + \frac{I_{ripple}^2}{12} \right] \times \frac{V_{out}}{V_{in}} - \frac{V_{out}^2}{V_{in}^2} \times I_{out}^2 \quad (24)$$

Now, the power dissipated by the input capacitor can be calculated by using the capacitor ESR.

$$P_{ci} = ESR_{in} I^2_{rmsci} \quad (25)$$

With $ESR_{in}$ = 166 mΩ, $V_{in}$ = 10 V, $V_{out}$ = 5 V, and $I_{out}$ = 1 A, the power dissipated is 59 mW (or 1.2% of the converter's output power). Likewise, the RMS current through the output capacitor ($I_{rmsco}$) is

$$I_{rmsco} = \sqrt{\frac{1}{12}} \times I_{ripple} \quad (26)$$

and the power dissipated is

$$P_{co} = ESR_{out} I^2_{rmsco} \quad (27)$$

Under the same conditions used for the input capacitor power calculation above, $P_{co}$ is 21 mW or 0.4%.

Now the input and output voltage ripple will be considered. Voltage ripple is caused by two effects, capacitor ESR times the ripple current, and the charge transfer divided by the capacitance.

$$V_{pkio} = ESR_{out} I_{ripple} \quad (28)$$

and

$$V_{RMSIO} = ESR_{out} I_{RMSCO} \quad (29)$$

where $V_{pkio}$ is the peak-to-peak output ripple voltage and $V_{rmsio}$ is the RMS output ripple voltage, both due to the output capacitor ESR. The peak-to-peak ripple voltage due to capacitance ($V_{pkqo}$) is

$$V_{pkqo} = \frac{1}{C_{out}} \times \frac{1}{2} \times \left[ \frac{1}{2 \times f} \times \frac{I_{ripple}}{2} \right] \quad (30)$$

Since the input ripple is somewhat harder to calculate, the input current is assumed to be larger than $I_{ripple}$. Under these conditions,

$$V_{pkii} = ESR_{in} \times \left[ I_{out} + \frac{I_{ripple}}{2} \right] \quad (31)$$

and

$$V_{pkqi} = \frac{1}{C_{in}} \times \frac{1}{f} \times \left[ 1 - \frac{V_{out}}{V_{in}} \right] \times I_{out} \times \frac{V_{out}}{V_{in}} \quad (32)$$

where $V_{pkii}$ in the input ripple's ESR component and $V_{pkqi}$ is the input ripple's capacitive component. Using worst-case conditions for the input and output ripple voltages ($V_{in}$ = 16.5 V, $I_{out}$ = 1.5 A, $ESR_{out}$ = 200 mΩ, and $C_{out}$ = 100 µF), $V_{rmsio}$ is 69 mV. Comparing the peak-to-peak ESR and capacitive ripples, respectively 238 mV and 69 mV, the capacitive component will not add enough voltage to make the RMS ripple exceed 80 mV. This is a high number, but still less than specified. A similar analysis of the voltage across the input capacitor reveals an expected RMS voltage at the input of less than 140 mV.

## SCHOTTKY DIODE

A Schottky diode is included in the circuit to prevent the internal diode of the n-channel MOSFET from turning on. The internal MOSFET should remain off for two reasons. First, being a silicon p-n diode, it has a reverse recovery charge that will cause an effect similar to shoot-through. To estimate these losses, the reverse recovery charge should be multiplied by the input voltage and the converter clock frequency. The charge can be estimated as 130% of half of the di/dt times the reverse recovery time squared. In this converter, with $V_{in}$ = 16.5 V and $I_{out}$ = 1.5 A, the loss would be about 130 mW or 2%. Note that while the n-channel MOSFET is causing this power loss, heat is generated in the p-channel MOSFET. The second reason that the Schottky is included is that it has a lower forward drop than the n-channel MOSFET internal diode. The Schottky diode conducts while both MOSFETs are off. During normal operation, this period totals about 300 ns per cycle. During a current limit caused by a very low load resistance, the inductor may completely discharge though the Schottky. The Schottky will generate much less heat than the MOSFET diode while the inductor is discharging.

The Schottky should be chosen so that its forward drop is less than the forward drop of the n-channel MOSFET internal diode at $I_{CLtherm}$. This selection will prevent the additional heat from reverse-recovery charge from overheating the p-channel MOSFET during a high current condition.

## FEEDBACK NETWORK DESIGN

A high-efficiency converter requires an output filter with low losses (a high Q). The fast 180-degree phase shift and large increase in gain at the filter resonant frequency complicate the design of the feedback network. For purposes of this discussion, the converter will be simplified to the behavioral model shown in Figures 3 and 4. The gain and phase of the output filter are given in Figure 5.

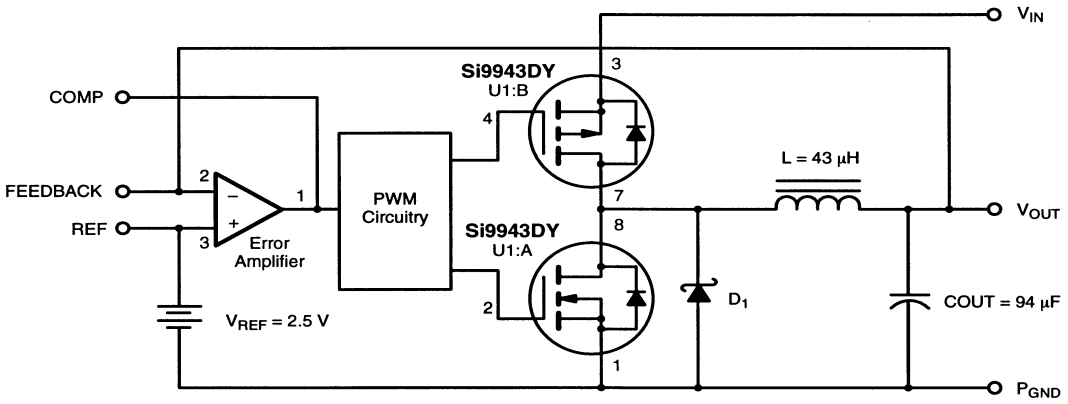



**FIGURE 3.** The Actual Circuit

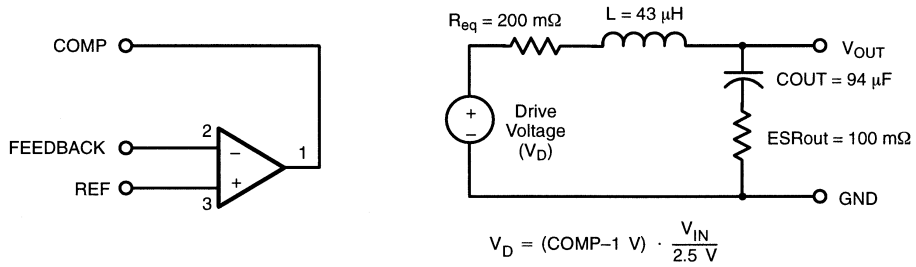



**FIGURE 4.** Behavioral Model for Feedback Loop Analysis

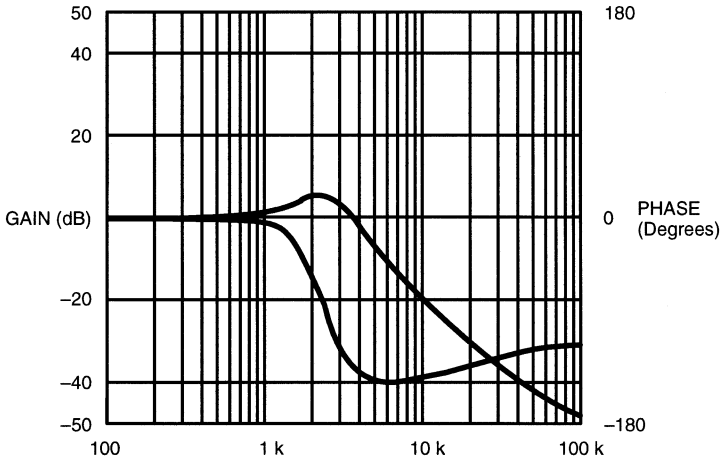



**FIGURE 5.** Output Filter Response

At low frequencies, the impedance of the inductor is small while the impedance of the capacitor is large, causing the output voltage to be about the same as the input voltage. At high frequencies, the inductor controls the current reaching the capacitor. The current through the inductor lags the input voltage by 90 degrees. Likewise, the voltage across the capacitor lags the current through the inductor by 90 degrees. Therefore, since the output voltage lags the input voltage by 180 degrees, the voltage is actually inverted by the filter.

Two approaches may be used for compensation of the buck converter power stage. Figures 6 and 7 show the low-performance (integrator) compensation method. The circuit values corresponding to these plots are as follows: $R_1$ = 150 kΩ, $C_1$ = 0.01 µF ($R_2$, $R_3$, $C_2$, and $C_3$ are not used). By using a dominant low-frequency pole the loop gain can be reduced to 0 dB at a frequency substantially below the filter resonant frequency. This results in a slow dynamic response.

To obtain better performance, the gain of the converter must be greater than one at the resonant frequency. We can achieve this improvement by designing the feedback circuit to differentiate, rather than integrate, near the resonant frequency. This approach, which is referred to as a lead-lag network, was used for the compensation of the buck converter. Figures 8 and 9 give the Bode plots for the feedback network and the total loop gain for the circuit values given in Figure 2.

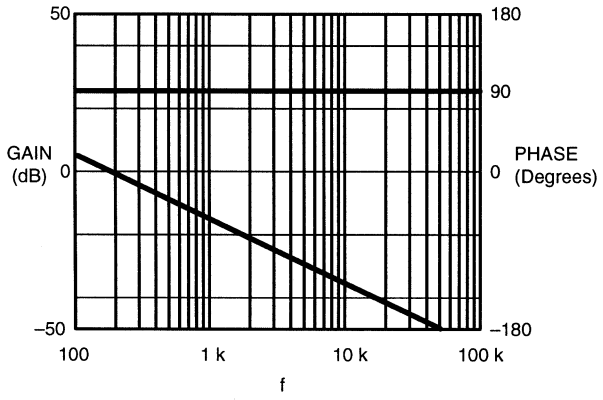



**FIGURE 6.** Low-performance Feedback Network Transfer Function

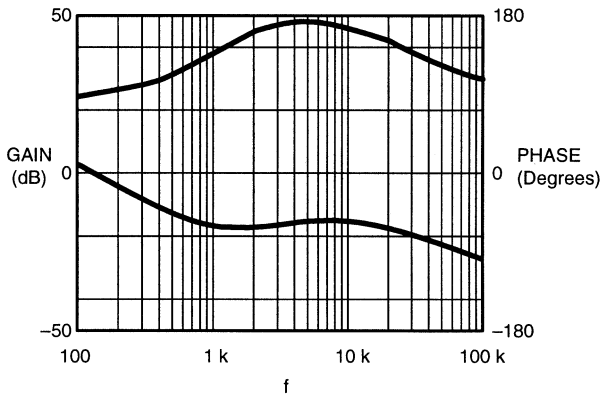



**FIGURE 8.** High-performance Feedback Network Transfer Function

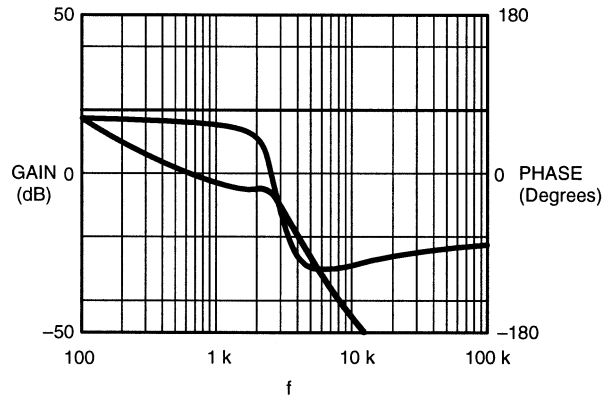



**FIGURE 7.** Open-loop Gain for the Converter with Low-performance Feedback Network

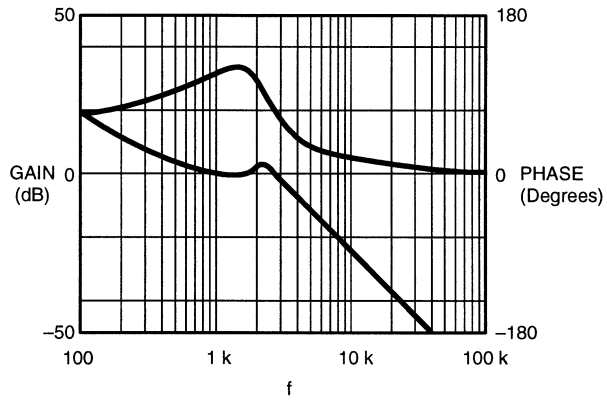



**FIGURE 9.** Open-loop Gain for the Converter with High-performance Feedback Network

## DYNAMIC RESPONSE LIMITATIONS

Synchronous operation of the converter ensures that the inductor flux is not left at zero, since the inductor current can flow in the reverse direction. Thus the converter runs in continuous conduction mode at all times. The minimum excursion of the output voltage which can be theoretically achieved in continuous conduction is limited by the output filter components.

Assuming an ideal feedback network, the controller responds to a step increase in load by immediately applying full voltage, $V_{in}$, to the output filter. Also assume that the output filter and switching circuit are lossless. Thus, using the behavioral model in Figures 3 and 4 with both resistors set to 0 Ω and solving for $V_{out}$, the following equations are obtained:

$$V_{in} - V_{out}(t) = L \times C \times \frac{d^2}{dt^2} \times V_{out}(t) \quad (33)$$

$$V_{ex}(t) = V_{out}(t) - V_{out}(0) \quad (34)$$

$$V_{ex}(0) = 0 \quad (35)$$

$$\frac{d}{dt} V_{ex}(t) I_o = \frac{-I_{step}}{C} \quad (36)$$

$$\frac{d^2}{dt^2} V_{ex}(t) I_o = \frac{V_{in} - V_{out}}{C \times L} \quad (37)$$

Solving equation 37 yields

$$V_{ex}(t) = \frac{-I_{step} \times \sin(\omega \times t)}{C \times \omega} + [V_{in} - V_{out}(0)][1 - \cos(wt)] \quad (38)$$

where

$$\omega = \sqrt{\frac{1}{L \times C}} \quad (39)$$

$V_{ex}(t)$ is at an extreme at $t_m$ as given by

$$t_m = \frac{\tan^{-1}\left[\frac{-I_{step}}{C \times \omega \times [V_{in} - V_{out}(0)]}\right]}{\omega} \quad (40)$$

Thus, for any given inductor, there is a minimum capacitor which must be used to achieve a given step response. This value should be padded by a factor of two if a high-performance compensation circuit is to be used. If a low-performance compensation circuit is to be used, the size of the capacitor will be even larger.

The error amplifier has a few characteristics which limit the feedback loop as well. First, the open loop gain is typically 75 dB. This is represented by a pole where the feedback network with an ideal op amp would reach a gain of 75 dB. Secondly, the op amp can source only about 1 mA. At a frequency and amplitude where more than 1 mA is required to keep the feedback pin at the reference voltage, the network will begin to resemble a wire, instead of an integrator. This should happen well above the unity gain crossover frequency of the control loop. Finally, the op amp has a limited gain bandwidth, as illustrated below in Figure 10.

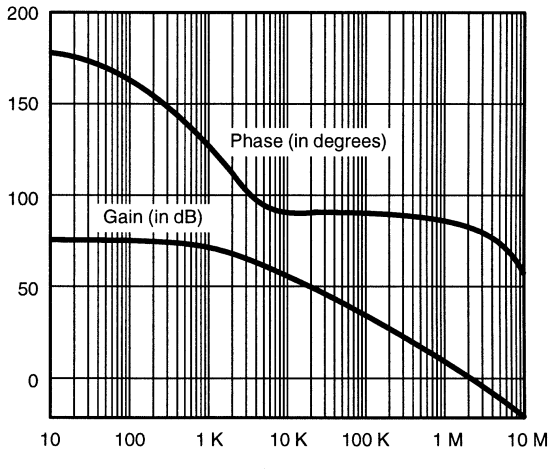



**FIGURE 10.** Error Amplifier Bode Plot

## SOFT-START CAPACITOR SELECTION

After the current limit has been triggered, the following sequence of events occurs. First, the EN and SS pins are pulled low by the current limit circuitry. Once the EN pin has shut off the Si9150CY, both Si9943DY MOSFETs are off. The EN resistor pulls up the EN pin at a rate determined by the EN capacitor ($C_6$ = 180 pF). Once EN passes its threshold voltage, the reference and the current source for the $\overline{\text{STBY}}$ pin are activated. After $\overline{\text{STBY}}$ passes its threshold, the current for $R_T$ and the feedback circuitry are turned on. After one clock cycle, the PWM circuitry is activated. Meanwhile, the error amplifier output is restricted to about 0.6 V above the SS voltage. Now the SS voltage ramps up, allowing the COMP voltage to increase. During this period, the converter output voltage will ramp up at a rate of approximately $V_{in}$/2.5 times the ramp rate of the SS voltage.

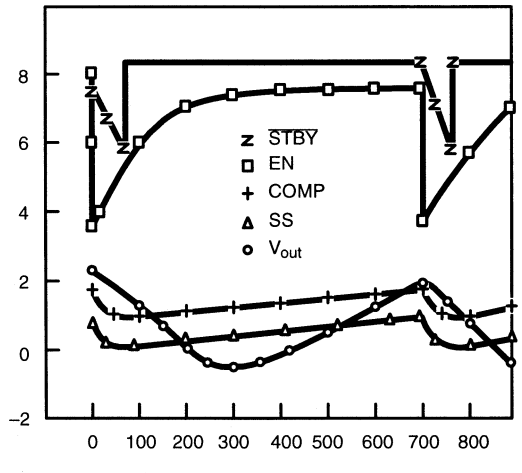



**FIGURE 11.** Startup Waveforms for $V_{in}$ = 8.2 V, $R_{LOAD}$ = Ω

Since the SS pin is pulled up by 25 µA (typical), the current needed to charge the output capacitor ($I_{startup}$) is

$$I_{startup} = C_{out} \times \frac{V_{in}}{2.5} \times \frac{25 \times 10^{-6}}{C_{ss}} \quad (41)$$

where $C_{SS}$ the value of the soft start capacitor in Farads. $I_{startup}$ should be limited to a value low enough so as not to trigger the current limit when combined with the load that the converter will see initially.

## LAYOUT CONSIDERATIONS

For stable PWM operation and reliable current limiting (i.e., no false trips), it is necessary to use bypass capacitors for the Si9150CY and to lay out the grounds properly. Also, for high-efficiency the high-current traces should be made wide to minimize parasitic losses. These layout-related topics are covered here.

The lossless current sense circuit uses the $V_{DD}$ pin as its reference. Therefore, the $V_{DD}$ pin of the Si9150CY should be tied directly to the source of the p-channel MOSFET. Since there is switching noise on the source of the p-channel MOSFET, the ground should be broken into logic ground and power ground as shown in Figure 12. The bypass capacitor for the Si9150CY should be tied to the logic ground. The connection between the power and logic grounds should be much longer than the $V_{DD}$ to p-channel source connection. As a result, the logic ground will track spikes on the p-channel source rather than the n-channel source. Of course, all the signal components, including the feedback network, should be referenced to the logic ground.

Figure 12 also shows the ac current paths. The most critical loop is defined by $C_9$, the p-channel MOSFET, and the n-channel MOSFET in parallel with $D_1$.

This loop should be kept very short to keep its resonant frequencies high, so that it will not be excited by the switching of the p-channel MOSFET.

There are two high-current dc paths whose trace resistances should be minimized, as shown in Figure 13. The figure also shows the RMS currents which must be carried by the input and output filter capacitors.

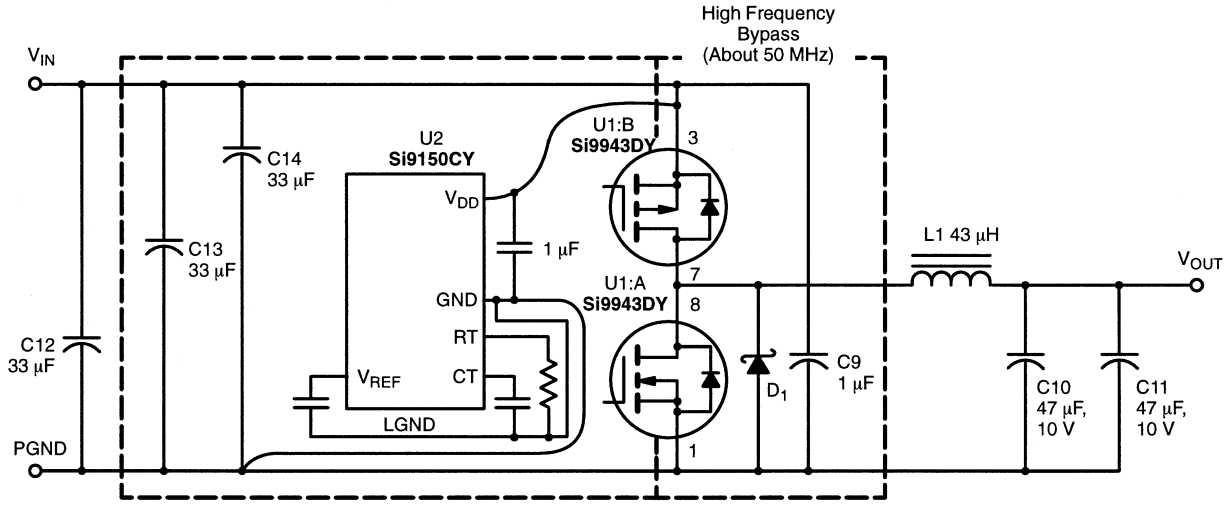


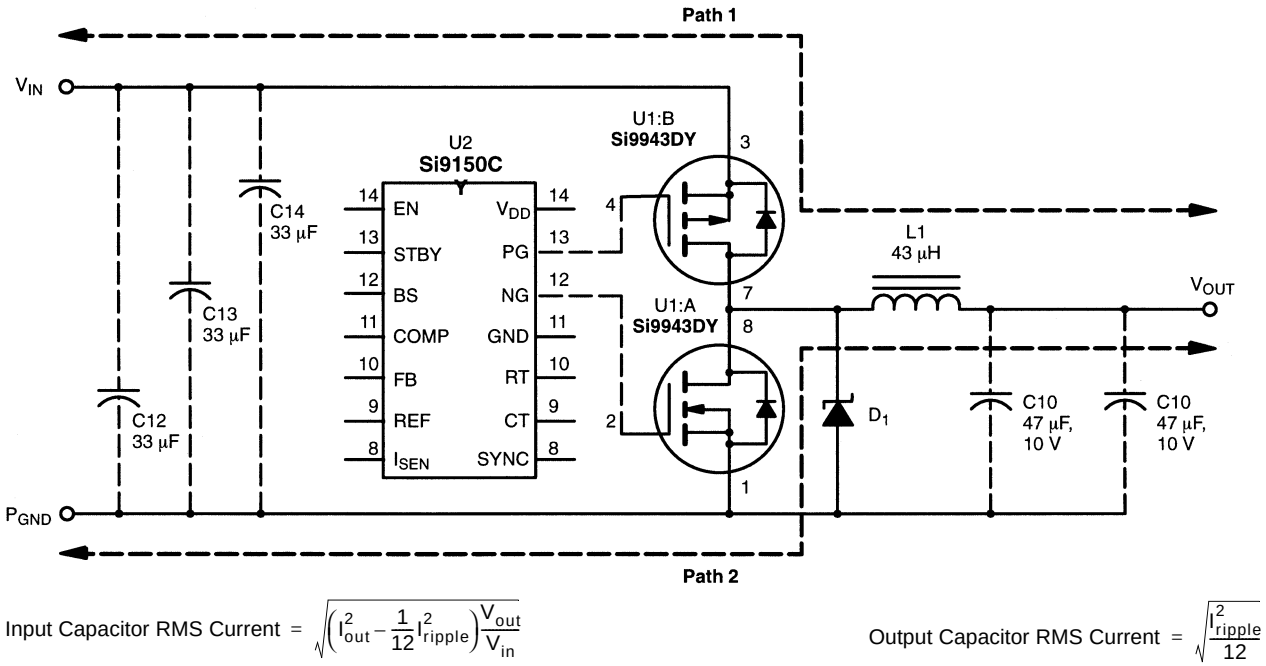

**FIGURE 12.** Ground Layout and High-frequency Bypassing

## CONCLUSION

Cost-effective and small dc-to-dc converters with greater than 90% efficiency no longer require exotic technologies. Figure 14 plots the efficiency versus load current for the converter design described above. Peak efficiency of 97% is achieved at $V_{in}$ = 6 V and $I_{out}$ = 400 mA. Over a broad range of line and load conditions the efficiency exceeds 90%. The converter efficiency was also measured for 3.3-V output (change $R_4$ from 33.2 kΩ to 105 kΩ), as shown in Figure 15. Peak efficiency is 94% at $V_{in}$ = 6 V and $I_{out}$ = 400 mA.

For both the 3.3-V and 5-V cases, the efficiency is reduced as $V_{in}$ increases. This reduction is due mainly to increased switching and inductor core losses and indicates that six NiCd or NiMH cells should be used for maximum efficiency .

The Si9150CY control IC integrates all of the required control functions for a synchronous rectified buck converter-including lossless current sensing, break-before-make timing, and PWM control functions. When driving the Si9943DY MOSFET half-bridge, an all surface-mount, 1.5-A buck regulator occupies only 2.25 square inches of circuit board.




Input Capacitor RMS Current $= \sqrt{\left(I_{out}^2 - \frac{1}{12} I_{ripple}^2\right)\frac{V_{out}}{V_{in}}}$

Output Capacitor RMS Current $= \sqrt{\frac{I_{ripple}^2}{12}}$

**FIGURE 13.** DC Current Paths

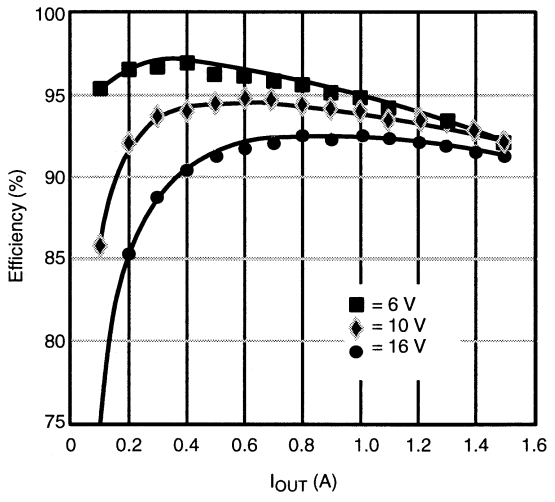



**FIGURE 14.** 5-V Output Buck Regulator Measured Efficiency

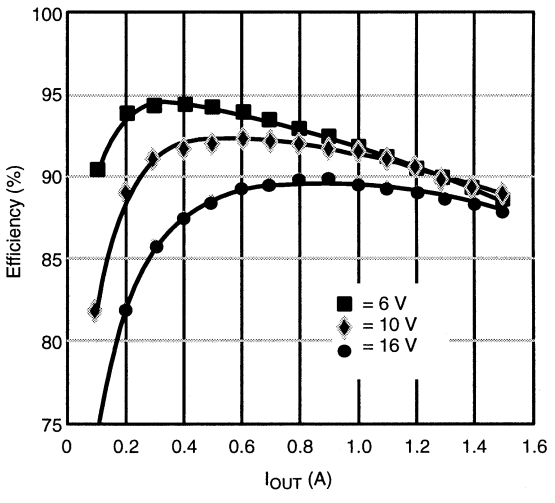



**FIGURE 15.** 3.3-V Buck Regulator Measured Efficiency